TPC R&D Proposal

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Abstract

We propose to begin research and development on the critical path items of a Time Projection Chamber (TPC) for the Electron Ion Collider (EIC). We will explore an innovative gating grid design to reduce ion backflow and to make quantitative comparisons among different gas multiplication methods. We will also begin small scale tests to evaluate the SAMPA ASIC being developed for ALICE to determine if this design will meet the requirements for the EIC, thereby reducing or eliminating the cost of a separate electronics design phase in the future.

1 Introduction

The Electron Ion Collider (EIC) will provide provide unprecedented access to gluon dynamics in nuclei at low x and high Q^2, and probe the spin content of the nucleus. For heavy Ion physicists this provides an opportunity to finally measure crucial aspects of the initial state needed to understand and model the evolution of the quark gluon plasma. The complete physics case for building the EIC is detailed in [1].

To prepare the way for the detectors at the EIC, and in response to an R&D called issued by Brookhaven National Laboratory in 2011, the EIC Tracking Consortium was formed and has begun work on critical path technologies anticipated to meet the anticipated EIC design requirements. In this document we review those requirements, discuss the benefits of including a Time Projection Chamber (TPC), and propose an R&D plan to address critical needs of an EIC TPC detector.

1.1 EIC Physics and Tracking Requirements

The current expected luminosity for the EIC is 10^{33} cm^{-2}s^{-1}, corresponding to a collision rate of 30–60 kHz, depending on the collision energy. The physics objectives require good tracking and identification of hadrons (π/K/p) at mid-rapidity, $-1 < y < 1$, and full azimuthal coverage up to ∼10 GeV. A momentum resolution of 1.5% or better at 5 GeV is required to measure the Upsilon [check source]. We adopt the standard convention with the z-direction aligned with the incident hadron. Acceptance for the scattered electron is needed at negative rapidities, extending to mid-rapidity for some physics processes, $-5 < y < 2$, extending out the beam momentum of the incident electron. The tracking and identification requirements for the scattered electron places severe constraints on the mass of the central tracking detector [quantify this]. For this reason, the TPC is preferred choice for the EIC central tracking detector. Although TPCs have been in use in high energy and nuclear physics experiments for more than 25 years, there is need for a focussed R&D effort at this time. The primary challenge is whether a TPC can handle the high rates at the EIC, and whether this can be done within a reasonable cost profile.

1.2 EIC TPC Specifications

The TPC radial dimension would be approximately 20-100 cm, with the inner radius set by the need to accommodate an inner vertex detector, and the outer radius set by the anticipated inner coil dimensions for a magnet with additional space Cerenkov particle identification detectors. The

longitudinal coverage of $-1 < \eta < 1$ leads to a length of approximately 2-meters. The magnetic field will be approximately 3 Tesla and the electric field will depend on the choice of drift gas, which is also linked to the details of the multiplication and readout.

The remaining design parameters have yet to be determined. One primary consideration is the need to reduce material along the electron direction, which may lead to single drift direction and fast gas, such as CF^4. However, meeting this goal will require understanding the nature of the ion back flow, and the dominant cost will be governed by the readout electronics. The research plan for FY15 will focus on these two areas.

2 TPC Research Plan

TPC R&D efforts have been discussed previously among the BNL and Yale groups within the EIC Tracking Consortium, with the ultimate goal of developing a prototype detector that would test the physics capabilities of such a detector. At this early stage of R&D, we have identified the ion backflow and electronics as two components that will heavily influence the design and cost of an EIC TPC.

The traditional method for reducing ion backflow in a TPC is to use a gating grid which when closed terminates the electric field lines above the readout plane, thereby inhibiting gas multiplication and limiting the buildup of positive ion space charge in the TPC. The gating grid limits the readout rate to the inverse of the sum of the electron drift time of the vessel and the ion drift time in the gating grid region. For a 2 meter chamber, electron drift times alone are in the range of 20–40 μs, which is on the edge of the anticipated average collision rate, but the addition of the ion drift time in the range of $[]\mu$s pushes the readout rate beyond this range. For the the ALICE TPC upgrade [2], which is striving for a similar collision rate of 50 kHz but much higher track densities, the standard gating grid is not an option, and multi-layered Gas Electron Multipliers (GEMs) are being developed to limit the ion backflow. For the lower track densities of the EIC, the situation is more nuanced, and a significant improvement to gating grid concept could make this option viable. Such an innovation was recently proposed by Howard Wieman during a review of the ALICE TPC upgrade. We propose to work with Howard Wieman on simulations and small scale bench tests to test this idea in the context of an EIC TPC as the first component of our R&D effort in 2015.

The second component is focused on the readout electronics. Historically, the cost of electronics procurements comprise between one third and one half the total cost of a TPC [3, 4]. The chip design process will drive these costs significantly higher, but these additional costs can be reduced or even eliminated by working with an existing chip design. The SAMPA chip, currently being developed for the ALICE TPC upgrade, is a third generation design that builds upon the PASA/ALTRO and S-ALTRO ASICs used by the STAR and ALICE TPCs. The SAMPA ASIC, which provides increased bandwidth and integration with reduced power, appears to be an optimal choice for an EIC TPC, but it is essential that we perform our own tests. By performing early tests and making contact with the SAMPA design team in Sao Paulo we will be able to influence the design in the event that changes are required. This group is about to begin its first component run in the fall of 2014. We propose to participate in the second phase ASIC run in order to procure a small sample of integrated ASICs for testing by the TPC Tracking Consortium.

2.1 Stacked Gating Grid R&D

The gating grid idea proposed by Howard Wieman is shown in Fig. 1. In this configuration, the conventional single layer gating grid is stacked four layers deep, enabling a larger fraction of the ions

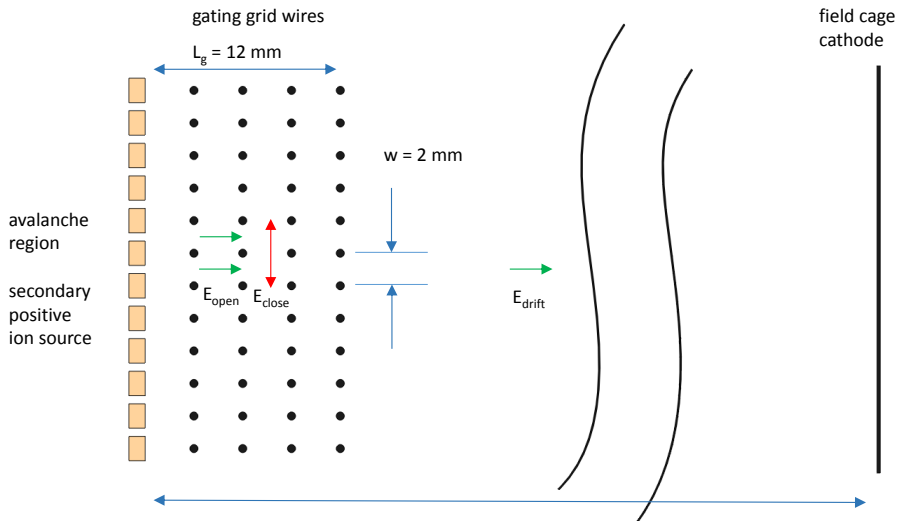

Figure 1: Schematic of stacked gating grid for reducing ion backflow in EIC TPC.

to be cleared in each cycle. This idea was proposed to supplement the multi-layer GEM readout in the ALICE TPC, but for the EIC one could consider reducing the number of GEM layers, using a single layer Micro-Mesh Gas Amplifiers (MicroMegas), or potentially using a conventional pad readout, depending on the efficacy of the new design. We propose to test this gating grid concept through simulations and small scale tests in the laboratory.

2.1.1 Simulations

To begin testing this gating grid concept, we will simulate the full electric field and layered gating grid performance using Garfield combined with Elmer or Magboltz. The simulations will be used to estimate field transparency, clearing time, ion leakage, and other operational parameters. This work will be performed by a postdoc at LLNL working 25% time under the guidance of Howard Wieman at LBNL. Results of the simulations will be used to guide experimental tests to be performed at the Weizmann Institute of Science.

2.1.2 Laboratory Tests

A small test chamber will be used to field test the layered gating grid design. These results will serve the benchmark the simulations, and will be used to estimate the impact of field distortions on the momentum resolution of the TPC. These measurements will also be compared to measurements for GEM and MicroMegas readouts. In general, the ion backflow might be governed by several parameters, namely: gas mixture, pressure, detector gain, hole diameter in case of GEM or lines per inch in case of MicroMegas, the combination of the drift, transfer and induction fields, number of GEMs used for the amplification element and asymmetry in the voltages applied across each GEM. The Heavy Ion Group at the Weizmann Institute of Science will perform the ion backflow measurements as a function of the parameters mentioned above.

2.2 SAMPA Electronics Development

The SAMPA ASIC design is led by the Sao Paulo group, which worked previously on the 16-channel PASA/ALTRO and S-ALTRO chips. SAMPA will integrate 32 channels of readout, beginning with positive/negative polarity Charge Sensitive Amplifiers that output semi-Gaussian voltage signals that are digitized by 10-bit 10 Msample/s ADCs. Signals are then processed digitally to remove distortions and transmitted over four 320 Mb/s e-links for a maximum rate of 1.28 Gbs. Details of the current SAMPA design are contained in [5].

The first run will deliver block components for the preamp, shaper, ADC, and DSP for testing by the Sao Paulo group. We propose to participate in the second run, procuring a small sample of integrated ASICs for use by the EIC TPC group. This run is expected to take place early in 2015. Testing will be overseen by a postdoc at LLNL who will supervise the graduate students at UC Davis who will perform actual testing. The full set of tasks for testing electronics is:

1. Work with electronics group to get packaged chips and associated documentation and board designs.
2. Build test boards and assemble with test chips.
3. Write software to interface with the chip.
4. Test the interface to the chip and exercise the functions.
5. Make quantitative measurements of the chip performance, power, noise, cross talk ,etc...
6. Report back to the electronics group and the EIC on the readiness of the chip design.

The budget request is limited to the cost of the parts and board assembly. Effort for the LLNL postdoc (25%) and UC Davis graduate student (50%) will be covered by existing base funding at their respective host institutions.

3 Personnel and Facilities

3.1 TPC Group at Weizman Institute of Science

The Heavy Ion Group at the Weizmann Institute of Science (WIS) has a long history and experience in designing and building the various gaseous detectors for CERN and RHIC heavy ion experiments. In particular this experience includes the TPC read-out chambers construction for the CERES/NA45 experiment at CERN SPS and GEM based Hadron Blind Detector for the PHENIX experiment at RHIC. In addition to the experience, the WIS group has a fully equipped lab, including the following items:

- laminar flow table inside our clean room
- recently build gas mixture system
- Scalable Readout System (SRS) purchased at CERN
- RCDAQ Linux based software for SRS developed at BNL
- CAEN High Voltage Main Frame and a number of power supplies
- 40 kV power supply for the TPC test cell
- NIM modules for a fast electronics
- all needed vacuum equipment including turbo pump

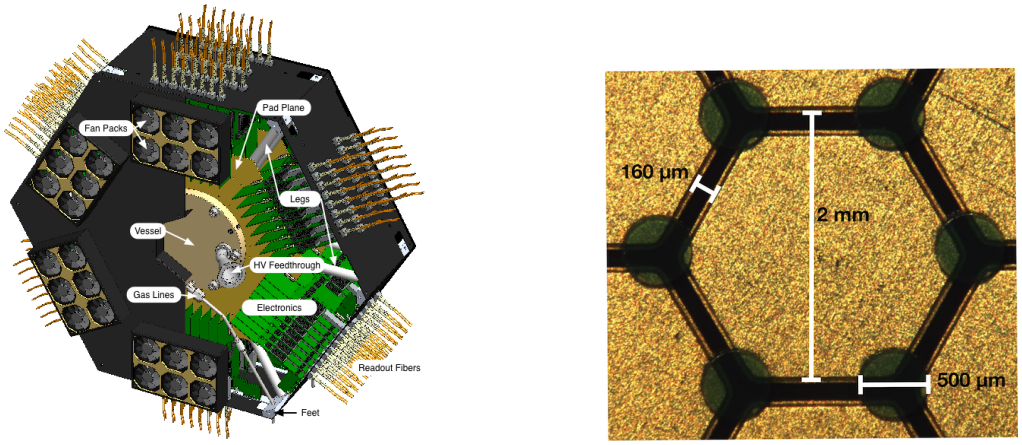

Figure 2: (Left) The NIFFTE fissionTPC with part of the cover removed. (Right) Micrograph of MicroMegas pad and pillar. The gold colored hexagon at the center is one pad and the close pack tessellation of the neighbor pads with 160 μm gaps between pads is also visible. The green circle at each hexagon point is a 75 μm tall insulating pillar to support the mesh.

The people from the Heavy Ion Group of the Weizmann Institute of Science who will work on this TPC R&D are Sasha Milov (Faculty), Ilia Ravinovich (Faculty), Sourav Tarafdar (PostDoc) and the number of summer students. Graduate students will also join this effort as it moves towards the design and construction of a prototype TPC for the EIC.

3.2 TPC Group at LLNL

The LLNL heavy ion group has significant experience in the design, construction, and operation of TPC detectors. The TPC lab at LLNL is fully equipped with a gas system, test vessel, and readout system. The group has experience in building MicroMegas and LEM gas gain systems, as well as the custom design of readout electronics [6]. The group has also developed software tools needed for calibration, tracking, and physics analysis. Past projects include a Hydrogen TPC for directional neutron detection [7] and a negative ion TPC with oxygen carrier that achieved single electron counting [8].

The LLNL TPC group is currently operating and analyzing data from a TPC in the Neutron Induced Fission Fragment Tracking Experiment (NIFFTE) [9]. The NIFFTE TPC is a two chamber MicroMegas TPC designed to make precision cross-section measurements at LANSCE. A cut-away of the TPC is shown in Fig. 3.2

3.3 TPC Collaborators

Howard Wieman, LBNL designed the STAR TPC [3], and has been an innovator in TPC design for many years. Howard will serve as a consultant on the simulations and bench tests of his layered gating grid design.

The UC Davis heavy ion group, led by Dan Cebra, has significant experience in all phases of TPC design, construction, calibration, and data analysis. The UC Davis group will contribute lab space and graduate student effort as needed to test and document the SAMPA ASICs.

4 Budget Justification

The WIS TPC group requires funding support for the mechanical design and technical support and in order to purchase the amplification detector elements for testing the layered gating grid, and measuring ion backflow compared to GEM and MicroMegas. Funding for the LLNL group will cover 25% postdoc effort for simulations of the layered gating grid. The remaining funding will be used to procure a small number of SAMPA ASICs, and to purchase and populate boards for testing. The full request and breakdown is listed in Table 1.

Task	Cost
Layered Gating Grid	**$75k**
simulation	$35k
mechanical design	$15k
technical support	$15k
detector components	$10k
SAMPA Testing	**$43k**
Mosis ASIC run	$35k
boards	$3k
parts assembly	$5k
Total	**$118k**

Table 1: Cost breakdown for FY15 TPC R&D.

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